In re Patent Application of
COFLER ET AL.
Serial No. **10/082,816**
Filed: **FEBRUARY 25, 2002**

REMARKS

Applicants thank the Examiner for the careful and thorough examination of the present application, for correctly withdrawing the previous rejection in view of Applicants' Appeal Brief, and for the indication of allowable subject matter. By this amendment, Claims 25, 26 and 30 are amended to eliminate an informality therein as noted by the Examiner. Claims 25-50 remain pending in the application. Favorable reconsideration is respectfully requested.

I. Summary of the Claimed Subject Matter

In general, the present invention is directed to a mechanism for handling branching instructions that allows an overall improvement in the branching latency, and applies particularly to a processor including decoupled architecture. According to the invention, with the processor core being clocked by a clock signal, a branching instruction received by the central unit in the course of a current cycle of the clock signal is processed in the course of the current cycle. The branching module is in the central unit, which makes it possible to process the branching instructions much more rapidly.

Referring to FIGs. 1 and 2, and pages 14-15 of the specification, for example, the presently claimed invention (as set forth in independent Claims 25, 36 and 38) will now be described.

Independent Claim 25 is directed to a method of handling branching instructions using a processor PROC

comprising a program memory PM storing program instructions, and a processor core CR comprising a plurality of processing units DU, AU and a central unit CU connected thereto, the central unit issuing instructions to the processing units based upon the program instructions. The method includes clocking the processor core with a clock signal, receiving a branching instruction in the course of a current clock cycle, and processing the received branching instruction in the course of the current clock cycle.

Independent Claim 36 is directed to a method of handling branching instructions using a processor PROC comprising a program memory PM storing program instructions, and a processor core CR comprising a plurality of processing units DU, AU and a central unit CU connected thereto, the central unit issuing instructions to the processing units based upon the program instructions, the method including receiving at the central core a branching instruction during a current clock cycle and processing the received branching instruction during the current clock cycle.

Independent Claim 38 is directed to a processor PROC comprising a program memory PM for storing program instructions and a processor core CR being clocked by a clock signal and comprising a plurality of processing units DU, AU and a central unit CU connected thereto. The central unit is for issuing instructions to the processing units based upon corresponding program instructions. The central unit includes a branching module BRU for receiving a branching instruction

during a current clock cycle, and processing this branching instruction during the current clock cycle.

II. The Claims are Patentable

Claims 25, 30, 36, 38 and 50 were rejected in view of Underwood et al. (U.S. Patent No. 5,928,357) taken alone or in combination with European Patent Application No. 1050805 for the reasons set forth on pages 3-9 of the Office Action. Claims 26-29, 31-35, 37 and 39-49 were indicated as being directed to allowable subject matter. Applicants contend that Claims 25, 30, 36, 38 and 50 clearly define over the cited references, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §102 and §103 is requested.

Independent method Claims 25 and 36 each set forth that a branching instruction received in the course of a current clock cycle of the clock signal is processed in the course of the current cycle. Independent processor Claim 38 includes a central unit for issuing instructions to the processing units based upon corresponding program instructions, and including a branching module for receiving a branching instruction during a current clock cycle, and processing this branching instruction during the current clock cycle. Thus, the branching module is in the central unit, which makes it possible to process the branching instructions much more rapidly. It is these combinations of features which are not fairly taught or suggested in the cited references and which patentably define over the cited references.

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The Underwood et al. patent is directed to a pipeline architecture which minimizes delays incurred during execution of branch instructions. While a first instruction is executing, a second instruction is fetched and is ready for execution at the beginning of the next clock cycle. Control logic examines the fetched instruction during the first clock cycle to determine whether the instruction is a branch instruction which may indicate that the address of the next instruction is not the next sequential address. Flags which indicate the state of the system are examined to determine if the address of the instruction is the next sequential address or the address indicated in the branch instruction.

Applicants agree with the Examiner that, in Underwood et al., the branch instruction and fetch of the next instruction is complete within one clock cycle. However, the Examiner has mischaracterized the newly cited reference as nothing in the reference teaches that the branching instruction is received by the central unit in the course of a current cycle of the clock signal and processed in the course of the current cycle.

As the Examiner is aware, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim.

The European patent application was cited to teach the use of a guard-indication register. Without discussing the details thereof, it is sufficient to note that nothing in such

reference discusses a branching instruction, received by the central unit in the course of a current cycle of the clock signal, is processed during the current cycle, as claimed. As such, this reference cannot make up for the deficiencies of the Emma et al. reference as discussed above.

There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Applicants maintain that the cited references do not disclose or fairly suggest the invention as set forth in Claims 25, 36 and 38. Furthermore, no proper modification of the teachings of these references could result in the invention as claimed. Thus, the rejections under 35 U.S.C. §102(b) and §103(a) should be withdrawn.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

III. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application

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can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone in order to resolve such informalities.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 2nd day of February, 2006.